



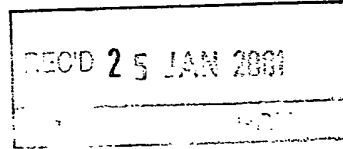
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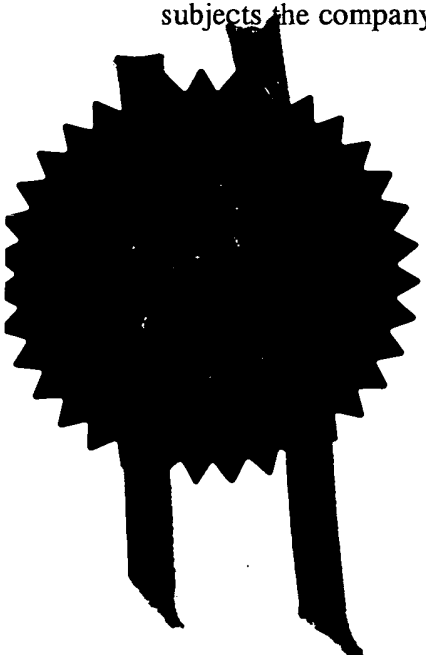
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4. Title of the invention

METHOD OF MANUFACTURING A THIN-FILM TRANSISTOR

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METHOD OF MANUFACTURING A THIN-FILM TRANSISTOR

This invention relates to a thin-film transistor (called TFT hereafter), and more specifically, relates to manufacturing technology for improving TFT transistor characteristics.

The various devices which use TFT's include an active matrix substrate of a liquid display device, for instance, which is formed on a transparent substrate such as glass as shown in Fig. 11 (A) and its roughly central region is identified as a picture display region 81. In this picture display region 81, picture elements are formed into sections by data lines 90 and scanning lines 91 composed of a metal film such as aluminum, tantalum, molybdenum, titanium and tungsten, a silicide film, a conductive semiconductor film, etc. In each picture element, a liquid crystal unit 94 (liquid crystal cell) is formed where picture signals are input through a TFT 30 for picture switching. For the data lines 90, a data-side drive circuit 60 is constructed that includes a shift register 84, a level shifter 85, video lines 87 and analog switches 86. For the scanning lines 91, scanning-side drive circuits 70 are constructed that have a shift register 88 and a level shifter 89. In each picture element, a holding capacitor 40 is formed between the scanning line 91 and a capacity line 92 extending parallel thereto, and the holding capacitor 40 has a function to improve the holding characteristics of charge at the liquid crystal units 94. This holding capacitor 40 is sometimes formed between the scanning line 91 of the front stage and a picture element electrode.

At the data-side and the scanning-side drive circuits 60 and 70, a CMOS circuit is constructed with an N type TFT 10 and a P type TFT 20 as shown in Fig. 11 (B). Such CMOS arrangement is used to implement an inverter circuit, etc. with more than one or two stages at the drive circuits 60 and 70.

Therefore, on the active matrix substrate 200, three types of TFTs are formed on the surface of the substrate that consist of an N type TFT 10 for the drive circuit, a P type TFT 20 for the drive circuit and an N type TFT 30 for picture element switching. However, these TFT 10, 20 and 30 have a common structure. Thus, in order to avoid redundancy of explanation, the structure of the N type TFT 10 for the drive circuit as well as the manufacturing method thereof will be explained with reference to Fig. 12, Fig. 13, Fig. 14 and Fig. 15.

As illustrated in Fig. 12, on the active matrix substrate 200, a bedding protective film 51 made of a silicon oxide film is formed at the surface side of the substrate 50. On the surface of this bedding protective film 51, a polycrystal semiconductor film 100 is formed that is patterned into island forms. On the surface of the semiconductor film 100, a gate insulating film 12 is formed, and a gate electrode 14 is formed on the surface of this gate insulating film 12. In the semiconductor film 100, a channel region 15 is formed at a region facing the gate electrode 14 through the gate insulating film 12. At the sides of this channel region 15, a high concentration source region 16 and a high concentration drain region 17 are formed in a self-aligned condition relative to the gate electrode 14. To the high concentration source region 16 and high concentration drain region 17, a source electrode 41 and a drain electrode 42 are respectively electrically connected through contact holes in an interlayer insulating film 52.

In order to manufacture the TFT 10 with such a structure, first, a substrate made of glass, etc. is cleaned by ultrasonic cleaning or the like as in Fig. 13 (A).

Next, as shown in Fig. 13 (B), a bedding protective film 51 is formed over the entire surface of the substrate 50 under the condition of a substrate temperature from about 150 to 450°C.

Next, as illustrated in Fig. 13 (C), a semiconductor film 100 is formed on the surface of the bedding protective film 51. At this time, by applying a low temperature process, the substrate 50 made of glass is prevented from being thermally deformed. The low temperature process indicates that the maximum temperature in the process (the maximum temperature wherein the temperature of a substrate as a whole increases at the same time) is lower than about 600°C (preferably, less than about 500°). On the contrary, a high temperature process indicates that the maximum temperature of the process (the maximum temperature wherein the temperature of a substrate increases as a whole at the same time) is higher than about 600°. This is to carry out a high temperature procedure at 700-1,200°C such as film-formation under high temperature and the thermal oxidation of silicon.

However, since it is impossible to form a polycrystal semiconductor film directly on the substrate in the low temperature process as explained later, this semiconductor film 100 should be crystallized after an amorphous semiconductor film 100 is formed first by a plasma

CVD method or a low pressure CVD method. As this crystallization method, for instance, methods such as a Solid Phase Crystallization (SPC) method and Rapid Thermal Annealing (RTA) method are included. As shown in Fig. 13 (D), by carrying out laser annealing wherein excimer laser beams using XeCl are irradiated (ELA: Excimer Laser Annealing/crystallization process), the rise in substrate temperature is restrained, and polycrystal Si with a large grain diameter is also provided.

In this crystallization process, laser beams (excimer laser) from a laser beam source 320, for example, are irradiated toward the substrate 50 that is placed on a stage 310 through an optical system 325 as shown in Fig. 14. In this process, line beams L0 wherein an irradiation range L is long in an X direction (for example, line beams at 200Hz of laser pulse cyclic frequencies) are irradiated onto the semiconductor film 100, and the irradiation region L is shifted in a Y direction. The beam length of the line beams L0 is 400mm herein, and the output intensity thereof is, for instance, 300mJ/cm². Also, in shifting the irradiation region L of laser beams in the Y direction, the line beams are scanned so as to overlap sections with 90% of the peak laser intensity in the width direction per region. As a result, the amorphous semiconductor film 100 is melted once, and is then polycrystallized after a cooling and solidifying process. In this process, the irradiation period of laser beams onto each region is extremely short and the irradiation region L is local relative to the substrate as a whole, so that the substrate 50 as a whole is not heated to a high temperature at the same time. Thus, even though the glass substrate used as the substrate 50 is inferior to a quartz substrate in heat resistance, there is no forming of deformation, cracks, etc. by heat.

Next, as shown in Fig. 13 (E), the polycrystal semiconductor film 100 is patterned in island forms by the photolithography technique.

Next, as illustrated in Fig. 15 (A), a gate insulating film 12 made of a silicon oxide film is formed at the surface side of the semiconductor film 100.

Next, as shown in Fig. 15 (B), a conductive film 140 containing aluminum, tantalum, molybdenum, titanium, tungsten, etc. is formed by a sputtering method.

Next, after forming a resist mask 301 on the surface of the conductive film 140 as shown in Fig. 15 (C), the conductive film 140 is patterned; and a gate electrode 14 is then formed as shown in Fig. 15 (D).

Next, as illustrated in Fig. 15 (E), phosphorus ions are introduced at a dosage of about e.g., $1 \times 10^{15} \text{cm}^{-2}$ onto the semiconductor film 100 with the gate electrode 14 as a mask. As a result, a source region 16 and a drain region 17 are formed in the semiconductor film 100 in a self-aligned condition relative to the gate electrode 14 and at a high impurity concentration of about $1 \times 10^{20} \text{cm}^{-3}$. The section in the semiconductor film 100 where the impurities are not introduced becomes a channel region 15.

Next, after forming an interlayer insulating film 52 as shown in Fig. 12, annealing is carried out for activation. Then, a source electrode 41 and a drain electrode 42 are formed after contact holes are formed in the interlayer insulating film 52.

In the N type TFT constructed as mentioned above, drain voltage that is positive relative to the potential of the source electrode 16 is applied to the drain electrode 42 as in Fig. 16 (A), and positive gate voltage is applied to the gate electrode 14. As a result, negative electric charge concentrates on the interface of the channel region 15 and the gate insulating film 12, forming an N type channel 151 (inversion layer). At this time, when drain voltage is small enough relative to gate voltage, the source region 16 and the drain region 17 are connected by the channel 151, so that drain electric current increases as drain voltage (non-saturation region) rises as indicated with a solid line L0 in the transistor characteristics (current-voltage characteristics) shown in Fig. 17. On the contrary, as drain voltage increases to almost equal to gate voltage, induced electron density near the drain region becomes small as shown in Fig. 16 (B), thus causing pinch-off. Under these conditions, even if drain voltage is increased higher than that level, drain electric current does not increase and becomes almost constant (at the saturation region) as indicated with the solid line L0 in Fig. 17. The current value in this case is called saturation current. Thus, if the TFT 10 is driven by applying this saturation region, constant drain current can be obtained, thus preventing the TFT 10 itself and peripheral circuits from being damaged by excess current.

As described above, the transistor characteristics of a TFT are basically dominated by the behavior of plural carriers (electrons in case of the N type, and holes in case of the P type).

However, when drain voltage becomes high, a phenomenon (Kink effect) is found wherein the above-noted drain current, which should be constant, abnormally increases. The reason will be explained below. First, as drain voltage becomes high and an electric field between the source and the drain intensifies at the TFT, carriers are accelerated by this electric field and will have large energy. The carriers are accelerated from the source region 16 towards the drain region 17, so that they will have the maximum energy near the drain region 17. The carriers with large energy (hot carriers) collide against the atoms in the semiconductor film and impurity atoms, thus generating pairs of electrons and holes. The generated holes, as shown in Fig. 16 (C), increase the potential of the channel region 15; and electric current in response to the injection of the holes mentioned above flows from the channel region 15 to the source region 16. Such a phenomenon can be considered by relating the channel region 15 to a base, the source region 16 to an emitter and the drain region 17 to a collector respectively. The electric current by holes flowing from the channel region 15 to the source region 16 can be considered as base current. The electric current flowing from the source region 16 to the drain region 17 in response to the electric current flowing from this channel region 15 to the source region 16 can be considered as collector electric current. Therefore, this phenomenon is also called bipolar action. With such bipolar transistor type behavior (bipolar action), even at the saturation region, drain current increases sharply (Kink effect) as drain voltage rises in the case of the conventional TFT as indicated with a two-dot chain line L1 in Fig. 17. As a result, there is a danger that the TFT 10 itself and the peripheral circuits would be damaged by excess current. In addition, such a phenomenon will be clear as the ON-state current level of the TFT 10 rises by increasing the degree of crystallization of the semiconductor film 100, so that the reliability tends to decline at a higher ON-state current level in case of the conventional TFT 10.

Therefore, the objectives of this invention are to reduce the bipolar transistor type behavior and to present a TFT manufacturing method that can stabilize saturation current and improve reliability.

In order to solve the problem mentioned above, in a method of manufacturing a thin-film transistor wherein a channel region facing a gate electrode through a gate insulating film and source and drain regions connected to the channel region are formed in a semiconductor film on the surface of an insulating substrate, this invention is characterized in that a

recombination center for capturing carriers is formed in the channel region by introducing impurities to the channel region.

In this invention, the impurities are at least one kind selected from the group consisting of e.g., inert gases, metals, Group III elements, Group IV elements and Group V elements.

The TFT manufactured by the method of this invention has a channel region 15 facing a gate electrode 14 through a gate insulating film 12 and source and drain regions 16 and 17 connected to the channel region 15 in a semiconductor film 100 formed on the surface of an insulating substrate 50 as shown in Fig. 16 (D), and this channel region 15 has a recombination center 150 for capturing a small number of carriers. In such TFT (for example, N type TFT), even if drain voltage becomes high and hole/electron pairs are generated by hot carriers, these holes and electrons are recombined and captured at the recombination center 150 formed in the channel region 15. As a result, as holes are injected into the source region 16 from the channel region 15, hole density would not become high, so that the injection of electrons from the source region 15 to the channel region is due to this hole-injection will not occur. Thus, there are no fluctuations in saturation current resulting from the bipolar transistor type behavior mentioned above. As a result, in the case of the TFT of this invention, as illustrated with a dotted line L2 or a one-dot chain line L3 in Fig. 17, drain current will not increase sharply even if drain voltage fluctuates at the saturation region. Thus, the TFT itself and peripheral circuits will not be damaged by excess current, etc., thus improving reliability.

In this invention, the process of introducing the impurities to a channel region is carried out by injecting impurities from a surface side of the channel region. Such a method is suitable for forming a recombination center on a surface side from the center in the direction of thickness of the channel region.

In this case, the process of introducing the impurities to a channel region is preferably carried out, after a crystallization process on a semiconductor film so as to form the channel region, by injecting impurities from a surface side of the channel region. In this way, this recombination center will not be dispersed or diminished by the crystallization process after the recombination center is formed.

In this invention, the process of introducing the impurities to a channel region may be carried out, after e.g., a crystallization process on a semiconductor film so as to form the channel region, by injecting impurities from a surface side of the channel region before a process of forming the gate electrode on a surface side of the channel region.

Also, the process of introducing the impurities to a channel region may be carried out, after the gate insulating film and the gate electrode are sequentially formed on a surface side of the channel region, by injecting impurities from a surface side of the gate electrode before an interlayer insulating film is formed on a surface side of the gate electrode.

In carrying out such a method, an average projected range of the impurities in the process of introducing impurities may be from the center in the direction of thickness of the channel region to an interface between the channel region and the gate insulating film.

Moreover, an average projected range of the impurities in the process of introducing impurities may be from the center in the direction of thickness of the channel region to an interface between the channel region and a layer located on the substrate side.

In this invention, the process of introducing the impurities to the channel region may be carried out by impurity diffusion from an impurity diffusion source arranged at a lower layer side of the channel region.

It is preferable that such impurity diffusion is carried out in a crystallization process on a semiconductor film so as to form the channel region.

In this invention, the crystallization process is laser annealing on a semiconductor film so as to form the channel region.

In this invention, each process carried out after introducing the impurities to the channel region is preferably carried out at a temperature below 400°, more preferably below 300°. In this way, this recombination center will not be thermally diffused or diminished after the recombination center is formed.

Embodiments of the invention will now be described by way of further example only and with reference to the accompanying drawings, in which:-

Fig. 1 is a cross-sectional view illustrating the structure of a TFT of embodiment 1 of the invention.

Figs. 2 (A) – (E) are cross-sectional views showing the manufacturing method of the TFT shown in Fig. 1.

Figs. 3 (A) – (D) are, in the manufacturing method of the TFT shown in Fig. 1, cross-sectional views showing each process that continues after the processes shown in Figs. 2.

Figs. 4 (A) – (C) are, in the manufacturing method of the TFT shown in Fig. 1, cross-sectional views showing each process that continues after the processes shown in Figs. 3.

Fig. 5 is a cross-sectional view illustrating the structure of a TFT of embodiment 2 of this invention.

Figs. 6 (A) – (C) are cross-sectional views showing the manufacturing method of the TFT shown in Fig. 5.

Figs. 7 (A) – (D) are, in the manufacturing method of the TFT shown in Fig. 5, cross-sectional views showing each process that continues after the processes shown in Figs. 6.

Figs. 8 (A) and (B) are cross-sectional views illustrating the structure of a TFT of embodiment 3 of this invention and a cross-sectional view showing the modified example thereof respectively.

Figs. 9 (A) – (F) are cross-sectional views showing the manufacturing method of the TFT shown in Fig. 8 (A).

Figs. 10 (A) – (E) are, in the manufacturing method of the TFT shown in Fig. 8 (A), cross-sectional views showing each process that continues after the processes shown in Figs. 9.

Fig. 11 (A) is a block diagram of an active matrix substrate for a liquid crystal display device, and Fig. 11 (B) is an equivalent circuit diagram of a CMOS circuit constructing the drive circuit thereof.

Fig. 12 is a cross-sectional view illustrating the structure of a conventional TFT.

Figs. 13 (A) – (E) are cross-sectional views showing the manufacturing method of the conventional TFT shown in Fig. 12.

Fig. 14 is a schematic block diagram of a laser annealing device used for laser annealing (crystallization process).

Figs. 15 (A) – (E) are, in the manufacturing method of the TFT shown in Fig. 12, cross-sectional views showing each process that continues after the processes shown in Figs. 13.

Figs. 16 (A) – (D) are diagrams for explaining the operation of a TFT.

Fig. 17 is a graph showing the transistor characteristics of TFTs of this invention, a conventional TFT and a model TFT.

Embodiments of the invention are explained with reference to figures. In any embodiment which will be explained below, a TFT is formed for picture-element switching or a drive circuit in an active matrix substrate for a liquid crystal display device, etc. Therefore, as described in the explanation of the prior art, three types of TFTs consisting of an N type TFT for a drive circuit, a P type TFT for a drive circuit and an N type TFT for picture-element switching should be formed on the same substrate. However, these TFTs have a common structure. Moreover, the TFT adopting this invention has a structure that is similar to that of the conventional TFT apart from the addition of the recombination center. Thus, in the following explanation, in order to avoid redundancy of explanation, the same reference numerals are used for the same elements as in the conventional TFT and for the manufacturing method thereof, and only the structure of an N type TFT for a drive circuit and the manufacturing method thereof will be explained.

Embodiment 1 (Example 1)

Fig. 1 is a cross-sectional view illustrating the structure of a TFT of embodiment 1 of the invention.

As shown in Fig. 1, in this embodiment, a bedding protective film 51 made of a silicon oxide film is formed on the surface side of a substrate 50, and an N type TFT 10 is formed on the surface of this bedding protective film 51. On the surface of this bedding protective film 51, a polycrystal semiconductor film 100 patterned in island forms is formed. On the surface of the semiconductor film 100, a gate insulating film 12 is formed, and a gate electrode 14 is formed on the surface of this gate insulating film 12. In the semiconductor film 100, a channel region 15 is formed at a region facing the gate electrode 14 through the gate insulating film 12. At the sides of this channel region 15, high concentration source region 16 and drain region 17 are formed in a self-aligned condition relative to the gate electrode 14. To the source region 16 and drain region 17, a source electrode 41 and a drain electrode 42 are electrically connected respectively through contact holes of an interlayer insulating film 52.

One section on the surface of the gate electrode 14 is hollow, and there is partially a thin section 141. This section 141 is for introducing impurities to a predetermined region of the channel region 15 in a manufacturing method described below.

In the TFT 10 constructed as above, a recombination center 150 is formed in the channel region 15 by impurities such as inert gases, metals, Group III elements, Group IV elements and Group V elements that are introduced to this channel region 15, or by crystal defects generated by the introduction of these impurities. The recombination center 150 concentrates on a location near the drain region 17 in the channel region 15 herein. In other words, the recombination center 150 concentrates on a region that is separated only by a distance equivalent to $1/3$ or $1/10$ of the channel length seen from the drain region 17.

In this embodiment, the density of the recombination center 150 is within a range from $1 \times 10^{13} \text{ cm}^{-3}$ to $1 \times 10^{20} \text{ cm}^{-3}$, and a carrier-capturing cross section at the recombination center 150 is within a range from $1 \times 10^{-13} \text{ cm}^2$ to $1 \times 10^{-20} \text{ cm}^2$. The carrier-capturing cross section and density of such a recombination center 150 can be controlled by a dosage of impurities into

the semiconductor film 100 (channel region 15) in the manufacturing method mentioned below.

Regarding the depth of the recombination center 150, it may be either a structure wherein the recombination center 150 concentrates on the side where the gate electrode 14 is located in the direction of thickness of the channel region 15, or a structure wherein the recombination center 150 concentrates on the side opposite to the side where the gate electrode 14 is located in the direction of thickness of the channel region herein; however, the recombination center 150 is formed so as to concentrate at a suitable location in response to the correlation between the thickness of the channel region 15 and the depth of a channel formed on the surface of this channel region 15, etc. The depth of the region where such a recombination center 150 concentrates can be controlled by acceleration voltage at the time of introducing impurities to the semiconductor film 100 (channel region 15), etc. in the manufacturing method mentioned later. In other words, it can be controlled by setting an average projected range during the injection of impurities to the semiconductor film 100, at the side of the gate electrode 14 or the side of the substrate 50 from the center in the direction of thickness of the channel-forming region 15.

The transistor characteristics (current-voltage characteristics) of the TFT 10 constructed as above are explained with reference to Fig. 1 and Fig. 17. Fig. 17 is a graph showing the results wherein the transistor characteristics of the TFTs of this invention, the conventional TFT and a model TFT are simulated. In Fig. 17, in the TFTs of this invention, the characteristics of TFTs - wherein the thickness of the semiconductor film 100 is 460 angstroms, channel length is $8\mu\text{m}$ and the recombination center 150 is formed at the length of $2\mu\text{m}$ from the location separated from the drain region 17 by $1\mu\text{m}$ - are expressed as a dotted line L2 and a one-dot chain line L3 respectively. Among these two TFTs, the TFT expressed as the dotted line L2 has the carrier-capturing cross areas of charged recombination center 150 and neutral recombination center 150 of $1 \times 10^{-13} \text{cm}^2$ and $1 \times 10^{-15} \text{cm}^2$ respectively. On the other hand, the TFT expressed as the one-dot chain line L3 has the carrier-capturing cross areas of charged recombination center 150 and neutral recombination center 150 of $1 \times 10^{-12} \text{cm}^2$ and $1 \times 10^{-14} \text{cm}^2$ respectively. The so-called charged recombination center 150 normally has negative electric charge and becomes neutral by capturing holes. On the other hand, the neutral recombination center 150 is normally neutral and charges positively by capturing

holes herein. Moreover, the density of the recombination center 150 of the TFTs expressed as either the dotted line L2 or the one-dot chain line L3 was set at $1 \times 10^{19} \text{cm}^{-3}$.

In the TFT 10 constructed as above, when drain voltage is much smaller than gate voltage, the source region 16 and the drain region 17 are connected by a channel, so that drain current increases as drain voltage rises (at the non-saturation region) as illustrated with a solid line L0 in Fig. 17.

Also, as drain voltage rises as high as the gate voltage, hole/electron pairs are formed by hot carriers. Formed holes are recombined and captured in the recombination center 150. Thus, many of the formed holes diminish in the channel region 15, so that the channel region 15 does not reach enough potential to inject holes into the source region 16. As a result, there will be no bipolar transistor type behavior (bipolar action) wherein electrons are injected into the channel region 15 from the source region 16 by the holes injected from the channel region 15 to the source region 16. Therefore, in case of the TFT 10 of this embodiment, as expressed with the dotted line L2 or the one-dot chain line L3 in Fig. 17, the Kink effect which sharply increases drain current at a saturation region can be restrained. As a result, by increasing the degree of crystallization of the semiconductor film 100, the TFT itself and peripheral circuits will not be damaged by excess current even if an ON-state current level or the like is raised, so that reliability can be also improved.

The method of manufacturing the TFT 10 having such a structure is explained with reference to Fig. 2, Fig. 3 and Fig. 4.

Fig. 2, Fig. 3 and Fig. 4 are all cross-sectional views illustrating the manufacturing method of the TFT of this embodiment.

In this embodiment, a substrate 50 made of glass, etc. cleaned by ultrasonic cleaning or the like is first prepared as shown in Fig. 2 (A).

Next, as shown in Fig. 2 (B), a bedding protective film made of a silicon oxide film or the like with a thickness of 2,000-5,000 angstroms is formed over the entire surface of the substrate 50 by a plasma CVD method under the condition of a substrate temperature from

about 150°C to 450°. A mixed gas of mono-silane and laughing gas, TEOS (tetraethoxysilane) and oxygen can be applied as the material gas.

Next, as illustrated in Fig. 2 (C), a semiconductor film 100 is formed on the substrate 50. At this time, the thermal deformation of the glass substrate 50 is prevented by applying a low temperature process. In other words, under the condition of a substrate temperature from about 150°C to 450°, a semiconductor film 100 made of an amorphous silicon film with a thickness of 300-700 angstroms is formed over the entire surface of the substrate 50 by a plasma CVD method. As the material gas, disilane or monosilane, for example, may be applied (film-forming process). In addition, as the method of forming the amorphous semiconductor film 100 on the substrate 50 under low temperature conditions, a vacuum CVD method, an EB deposition method, a sputtering method or the like may be used instead of the plasma CVD method.

Next, as shown in Fig. 2 (D), laser beams are irradiated onto the semiconductor film 100, thus carrying out laser annealing (crystallization process). In this crystallization process, line beams L0 are irradiated onto the semiconductor film 100 and the irradiation region L is shifted to a Y direction as explained with reference to e.g. Fig. 14.

Next, as shown in Fig. 2 (E), the polycrystal semiconductor film 100 is patterned in island forms by applying a photolithography technique.

Next, as shown in Fig. 3 (A), a gate insulating film 12 made of a silicone oxide film with a thickness of 600-1,500 angstroms is formed on the side of the surface by a plasma CVD method with TEOS (tetraethoxysilane) or oxygen gas as a material gas.

Next, as illustrated in Fig. 3 (B), a conductive film 140 containing aluminum, tantalum, molybdenum, titanium, tungsten, etc. is formed by a sputtering method.

Next, as shown in Fig. 3 (C), after forming a resist mask 301 on the surface of the conductive film 140, the conductive film 140 is patterned and a gate electrode 14 is formed as shown in Fig. 3 (D).

Next, as shown in Fig. 4 (A), a resist mask 302 is formed, by a photolithography technique, that has an opening section 303 at a location near the drain region 17 on the upper layer side of the channel region 15, for example, in a region separated only by a distance equivalent to $1/3$ - $1/10$ of a channel length seen from the drain region 17.

Next, shallow etching is partially carried out on the surface of the gate electrode 14 through the resist mask 302. As a result, as shown in Fig. 4 (B), out of the surface of the gate electrode 14, only the region that is separated just by a distance equivalent to $1/3$ - $1/10$ of a channel length seen from the drain region 17 is etched, and a thin section 141 is formed partially in the gate electrode 14.

Next, as illustrated in Fig. 4 (C), phosphorus ions are introduced at a dosage of about $1 \times 10^{19} \text{cm}^{-3}$ to the semiconductor film 100 with the gate electrode 14 as a mask. As a result, source region 16 and drain region 17 at a high impurity concentration of about $1 \times 10^{20} \text{cm}^{-3}$ are formed in the semiconductor film 100 in a self-aligned condition relative to the gate electrode 14. In this case, the section of the semiconductor film 100 where no impurities are introduced becomes a channel region 15.

Also, even from the thin section 141 of the gate electrode 14, phosphorus ions are injected into the semiconductor film 100 (channel region 15). However, the amount of impurities injected from the thin section 141 of the gate electrode 14 is small since the gate electrode 14 becomes a blocking layer. Therefore, impurities are introduced to a region equivalent to the thin section 141 of the gate electrode 14 in the semiconductor film 100 (channel region 15) in a smaller amount than that to the source region 16 and the drain region 17, and a recombination center explained with reference to Fig. 1 is then formed.

Next, as shown in Fig. 1, after an interlayer insulating film 52 is formed on the surface side of the gate electrode 14, annealing for activation is carried out under the temperature condition of 400° , preferably lower than 300° . Thereafter, a source 41 and a drain electrode 42 are formed after contact holes are formed in the interlayer insulating film 52. As a result, a TFT 10 is formed.

Thus, in the manufacturing method of this embodiment, the process of introducing impurities to the channel region 15 is carried out by the injection of impurities from the

surface side of the channel region 15 (semiconductor film 100), so that it is suitable for concentrating the recombination center 150 on the side where the gate electrode 14 is located in the direction of thickness of the channel region 15.

Also, in this embodiment, the process of forming the recombination center 150 by introducing impurities to the semiconductor film 100 is carried out after the recrystallization process (laser annealing) on the semiconductor film 100 for forming the channel region 15, so that the semiconductor film 100 is not exposed to a high temperature atmosphere that is greater than e.g., 400° (preferably 300°). Thus, the impurities introduced to the semiconductor film 100 (channel region 15) for forming a recombination center will not be inappropriately thermally diffused, or the defects formed by the introduction of impurities (recombination center 150) will not be fixed.

Moreover, in the above-noted embodiment, the introduction of impurities to form a source and drain region was carried out at the same time with the introduction of impurities to form a recombination center; however, they may be carried out in separate processes. The procedural order of forming a thin section 141 partially in a gate electrode 14 after forming source and drain electrodes, and then forming a recombination center, for example, may be adopted.

In this case, ions such as inert gases and metals can be freely selected as ions for forming a recombination center. This is because ions can be injected only into a channel region corresponding to the locally thin section 141 with the source and drain regions as masks. Moreover, after injecting ions for forming source and drain regions, the injection of ions so as to form a recombination center can be carried out after a heat treatment for activation. In this case, defects formed by lowering process treatments thereafter will not recover, so that a recombination center can be formed efficiently.

Embodiment 2 (Example 2)

Fig. 5 is a cross-sectional view illustrating the structure of a TFT of embodiment 2 of this invention.

As shown in Fig. 5, a bedding protective film 51 made of a silicon oxide film is also formed on the surface side of a substrate 50 in this embodiment, and a TFT 10 is formed on the surface thereof. The fundamental structure of this TFT 10 is the same as that of the TFT 10 which was explained with reference to Fig. 1, except that a gate electrode 14 has an equal film thickness. In other words, in a polycrystal semiconductor film 100 that was patterned in island forms, a channel region 15 facing a gate electrode 14 through a gate insulating film 12, a source electrode 16 connected to the channel region 15 and a drain region 17 connected to the channel region 15 on the side opposite this source region 16 are formed. Other components are the same as those in the TFT 10 of the embodiment 1, so that the same reference numerals are used for the corresponding sections and the explanations are omitted.

Also in this embodiment, in the TFT 10 constructed as above, a recombination center 150 is formed in the channel region 15 by impurities such as inert gases, metals, Group III elements, Group IV elements and Group V elements introduced to this channel region 15, or by crystal defects generated by the introduction of these impurities. The recombination center 150 concentrates on a location near the drain region 17 in the channel region 15 herein. In other words, the recombination center 150 concentrates on a region that is separated only by a distance equivalent to $1/3$ or $1/10$ of the channel length seen from the drain region 17.

Also in this embodiment, the density of the recombination center 150 is within a range from $1 \times 10^{13} \text{ cm}^{-3}$ to $1 \times 10^{20} \text{ cm}^{-3}$, and a carrier-capturing cross section at the recombination center 150 is within a range from $1 \times 10^{-13} \text{ cm}^2$ to $1 \times 10^{-20} \text{ cm}^2$. Also, even in this embodiment, it may be either a structure wherein the recombination center 150 concentrates on the side where the gate electrode 14 is located in the direction of thickness of the channel region 15, or a structure wherein the recombination center 150 concentrates on the side opposite to the side where the gate electrode 14 is located in the direction of thickness of the channel region; however, the recombination center 150 is formed so as to concentrate at a suitable location in response to the correlation between the thickness of the channel region 15 and the depth of a channel formed in this channel region 15.

In the TFT 10 constructed as above, when the drain voltage rises as high as the gate voltage, hole/electron pairs are formed by hot carriers. In this embodiment, the formed holes are recombined and then captured at the recombination center 150. Thus, many of the formed holes diminish in the channel region 15, so that the channel region 15 does not reach enough

potential to inject holes into the source region 16. As a result, there will be no bipolar transistor type behavior wherein electrons are injected into the channel region 15 from the source region 15 by the holes injected from the channel region 15 to the source region 16. Therefore, in case of the TFT 10 of this embodiment, as expressed with the dotted line L2 or the one-dot chain line L3 in Fig. 17, the Kink effect which sharply increases drain current at a saturation region can be restrained. As a result, by increasing the degree of crystallization of the semiconductor film 100, the TFT itself and peripheral circuits will not be damaged by excess current even if an ON-state current level or the like is raised, so that reliability can also be improved.

The method of manufacturing the TFT 10 having such a structure is explained with reference to Fig. 6 and Fig. 7. Fig. 6 and Fig. 7 show cross-sectional views illustrating the manufacturing method of the TFT of this embodiment. In addition, in the manufacturing method of the TFT 10 of this embodiment, the procedures up until the polycrystal semiconductor film 100 is formed are the same as the processes explained with reference to Fig. 2 (A) – Fig. 2 (E) in the TFT manufacturing method of embodiment 1. In other words, as shown in Fig. 2 (B), a bedding protective film 51 is under the condition of a substrate temperature from about 150°C to 450°. Then, after a semiconductor film 100 made of an amorphous silicon film is formed over the entire surface of the substrate 50 under the condition of a substrate temperature from about 150°C to 450°C as illustrated in Fig. 2 (C), the semiconductor film 100 is polycrystallized by laser annealing with the irradiation of laser beams to the semiconductor film 100 as shown in Fig. 2 (D), and thereafter, the polycrystal semiconductor film 100 is patterned in island forms by a photolithography technique as shown in Fig. 2 (E).

Next, as shown in Fig. 6 (A), a gate insulating film 12 made of a silicon oxide film with a thickness of 600-1,500 angstroms is formed on the side of the surface by plasma CVD method with TEOS (tetraethoxysilane) or oxygen gas as a material gas.

Next, as illustrated in Fig. 6 (B), a resist mask 305 is formed, by a photolithography technique, that has an opening section 304 at a location near the drain region 17 at the upper layer side of the channel region 15, for example, at a location separated only by a distance equivalent to 1/3-1/10 of a channel length seen from the drain region 17.

Next, as shown in Fig. 6 (C), impurities such as inert gases, metals, Group III elements, Group IV elements and Group V elements are introduced to the semiconductor film 100 through the opening section of the resist mask. As a result, in the semiconductor film 100 (channel region 15), the impurities are introduced to the region equivalent to the opening section 304, so that a recombination center 150 is formed by the impurities or the defects formed by the introduction of the impurities.

Next, as illustrated in Fig. 7 (A), a conductive film 140 containing aluminum, tantalum, molybdenum, titanium, tungsten, etc. is formed by a sputtering method.

Next, as shown in Fig. 7 (B), after forming a resist mask 301 on the surface of the conductive film 140, the conductive film 140 is patterned and a gate electrode 14 is formed as shown in Fig. 7 (C). Then, as shown in Fig. 7 (D), phosphorus ions are introduced at a dosage of about $1 \times 10^{15} \text{cm}^{-2}$ to the semiconductor film 100 with the gate electrode 14 as a mask. As a result, source region 16 and drain region 17 at the high impurity concentration of about $1 \times 10^{20} \text{cm}^{-3}$ are formed in the semiconductor film 100 in a self-aligned condition relative to the gate electrode 14.

Next, as shown in Fig. 5, after an interlayer insulating film 52 is formed on the surface side of the gate electrode 14, annealing for activation is carried out below 400° , preferably below 300° . Thereafter, source 41 and drain electrodes 42 are formed after contact holes are formed in the interlayer insulating film 52. As a result, a TFT 10 is formed.

Thus, even in this embodiment, the process of introducing impurities to the channel region 15 is carried out by the injection of impurities from the surface side of the channel region 15 (semiconductor film 100), so that it is suitable for concentrating the recombination center 150 on the side where the gate electrode 14 is located in the direction of thickness of the channel region 15.

Also, in this embodiment, the process of forming the recombination center 150 by introducing impurities to the semiconductor film 100 is carried out after the recrystallization process (laser annealing) on the semiconductor film 100 for forming the channel region 15, so that the semiconductor film 100 is not exposed to a high temperature atmosphere greater than e.g., 400°C (preferably 300°). Thus, the impurities introduced to the semiconductor film 100

(channel region 15) for forming a recombination center will not be inappropriately thermally diffused, or the defects formed by the introduction of impurities (recombination center 150) will not be fixed.

Embodiment 3 (Example 3)

Fig. 8 (A) is a cross-sectional view illustrating the structure of a TFT of embodiment 3 of the invention.

As shown in Fig. 8 (A), a bedding protective film 51 made of a silicone oxide film is also formed on the surface side of a substrate 50 in this embodiment, and a TFT 10 is formed on the surface thereof. The fundamental structure of this TFT 10 is the same as that of the TFT 10 which was explained with reference to Fig. 1, except that a semiconductor film 11 for bedding is formed at a lower layer side of the semiconductor film 100 constructing active layers. In other words, as shown in Fig. 8 (A), in a polycrystal semiconductor film 100 that was patterned in island forms, a channel region 15 facing a gate electrode 14 through a gate insulating film 12, a source electrode 16 connected to the channel region 15 and a drain region 17 connected to the channel region 15 on the side opposite this source region 16 are formed. Other components are the same as those in the TFT 10 of the embodiment 1, so that the same reference numerals are used for the corresponding sections and explanations are omitted.

Also in this embodiment, in the TFT 10 constructed as above, a recombination center 150 is formed in the channel region 15 by impurities such as inert gases, metals, Group III elements, Group IV elements and Group V elements introduced to this channel region 15, or by crystal defects generated by the introduction of these impurities. The recombination center 150 concentrates on a location near the drain region 17 in the channel region 15 herein. In other words, the recombination center 150 concentrates on a region that is separated only by a distance equivalent to 1/3 or 1/10 of the channel length seen from the drain region 17.

Also in this embodiment, the density of the recombination center 150 is within a range from $1 \times 10^{13} \text{cm}^{-3}$ to $1 \times 10^{20} \text{cm}^{-3}$, and a carrier-capturing cross section at the recombination center 150 is within a range from $1 \times 10^{-13} \text{cm}^2$ to $1 \times 10^{-20} \text{cm}^2$.

Also, even in this embodiment, it may be either a structure wherein the recombination center 150 concentrates on the side where the gate electrode 14 is located in the direction of thickness of the channel region 15, or a structure wherein the recombination center 150 concentrates on the side opposite the side where the gate electrode 14 is located in the direction of thickness of the channel region; however, the recombination center 150 is formed so as to concentrate at a suitable location in response to the correlation between the thickness of the channel region 15 and the depth of a channel formed in this channel region 15. The depth of the region where such a recombination center 150 concentrates can be controlled by the diffusion conditions of impurities from an impurity introducing region 111 (impurity diffusion source) of the bedding semiconductor film 11 to the semiconductor film 100 (channel region 15).

In the TFT 10 constructed as above, when the drain voltage rises as high as the gate voltage, hole/electron pairs are formed by hot carriers. In this embodiment, the formed holes are recombined and then captured at the recombination center 150. Thus, many of the formed holes diminish in the channel region 15, so that the channel region 15 does not reach enough potential to inject holes into the source region 16. As a result, there will be no bipolar transistor type behavior wherein electrons are injected into the channel region 15 from the source region 16 by the holes injected from the channel region 15 to the source region 16. Therefore, in case of the TFT 10 of this embodiment, as expressed with the dotted line L2 or the one-dot chain line L3 in Fig. 17, the Kink effect which sharply increases drain current at a saturation region can be restrained. As a result, by increasing the degree of crystallization of the semiconductor film 100, the TFT itself and peripheral circuits will not be damaged by excess current even if an ON-state current level or the like is raised, so that reliability can also be improved.

The method of manufacturing the TFT 10 having such a structure is explained with reference to Fig. 9, Fig. 10 and Fig. 11.

Fig. 9, Fig. 10 and Fig. 11 are cross-sectional views illustrating the manufacturing method of the TFT of this embodiment.

Also, in this embodiment, a substrate 50 made of glass, etc. cleaned by ultrasonic cleaning or the like is first prepared as shown in Fig. 9 (A).

Next, as shown in Fig. 9 (B), a bedding protective film made of a silicon oxide film or the like with a thickness of 2,000-5,000 angstroms is formed over the entire surface of the substrate 50 by a plasma CVD method under the condition of a substrate temperature from about 150°C to 450°.

Also, a bedding semiconductor film 11 is formed on the surface of a bedding protective film 51. No crystallization is required for this bedding semiconductor film 11, so that it is formed by the low temperature process.

Next, as shown in Fig. 9 (C), a resist mask 307 is formed, by a photolithography technique, that has an opening section 306 at a location near the drain region 17 at the upper layer side of the channel region 15, for example, in a location separated only by a distance equivalent to 1/3-1/10 of a channel length seen from the drain region 17.

Next, through the opening section 306 of the resist mask 307, impurities consisting of inert gases, metals, Group III elements, Group IV elements or Group V elements are injected into the bedding semiconductor film 11. As a result, in the bedding semiconductor film 11, the impurities are introduced to a region equivalent to the opening section 306, thus forming an impurity introducing region 111 (impurity diffusion source).

Next, as illustrated in Fig. 9 (D), a semiconductor film 100 made of an amorphous silicon film with a thickness of 300-700 angstroms is formed by a plasma CVD method on the surface of the bedding semiconductor film 11 formed on the substrate 50 under the condition of a substrate temperature from about 150°C to 450°.

Next, as shown in Fig. 9 (E), laser beams are irradiated onto the semiconductor film 100, thus carrying out laser annealing (crystallization process). In this crystallization process, line beams L0 are irradiated onto the semiconductor film 100 and the irradiation region L is shifted to the Y direction as explained with reference to e.g. Fig. 14.

As a result, the impurities that were introduced to the impurity introducing region 111 of the bedding semiconductor film 11 thermally diffuse from the bedding semiconductor film 11 to the semiconductor film 100, and a recombination center 150 is formed.

Next, as shown in Fig. 9 (E), the polycrystal semiconductor film 100 is patterned in island forms by applying a photolithography technique. At this time, the bedding semiconductor film 11 is also patterned.

Next, as shown in Fig. 10 (A), a gate insulating film 12 made of a silicon oxide film with a thickness of 600-1,500 angstroms is formed on the surface side of the semiconductor film 100 by a plasma CVD method with TEOS (tetraethoxysilane) or oxygen gas as a material gas.

Next, as illustrated in Fig. 10 (B), a conductive film 140 containing aluminum, tantalum, molybdenum, titanium, tungsten, etc. is formed by a sputtering method.

Next, as shown in Fig. 10 (C), after forming a resist mask 301 on the surface of the conductive film 140, the conductive film 140 is patterned and a gate electrode 14 is formed as shown in Fig. 10 (D).

Next, as illustrated in Fig. 10 (E), phosphorus ions are introduced at a dosage of about $1 \times 10^{15} \text{cm}^{-2}$ to the semiconductor film 100 with the gate electrode 14 as a mask. As a result, source region 16 and drain region 17 at high impurity concentration of about $1 \times 10^{20} \text{cm}^{-3}$ are formed in the semiconductor film 100 in a self-aligned condition relative to the gate electrode 14. In this case, the section where no impurities are introduced becomes a channel region 15.

Next, as shown in Fig. 8 (A), after an interlayer insulating film 52 is formed on the surface side of the gate electrode 14, annealing for activation is carried out below 400°C , preferably below 300°C . Thereafter, source 41 and a drain electrode 42 are formed after contact holes are formed in the interlayer insulating film 52. As a result, a TFT 10 is formed.

Thus, in this embodiment, the process of introducing impurities to the channel region 15 is carried out by the impurity diffusion from the impurity introducing region 111 (impurity diffusion source) of the bedding semiconductor film 11 deposited at the lower layer side of the channel region 15 (semiconductor film 100), so that it is suitable for concentrating the recombination center 150 on the side opposite (the side of the substrate 50) the side where the gate electrode 14 is located in the direction of thickness of the channel region 15.

Also, in this embodiment, the recombination center 150 is formed at the same time with the recrystallization process (laser annealing) on the semiconductor film 100 for forming the channel region 15; and after this process, it is not exposed to a high temperature atmosphere. In other words, after the recombination center 150 is formed, it is not exposed to temperature higher than 400°C (preferably 300°C). Thus, the impurities introduced to the channel region 15 (semiconductor film 100) for forming a recombination center will not be inappropriately thermally diffused, or the defects formed by the introduction of impurities (recombination center 150) will not be fixed.

Moreover, in this embodiment, the impurity introducing region 111 formed by the injection of impurities to the bedding semiconductor film 11 is the impurity diffusion source; however, as shown in Fig. 8 (B), the section wherein impurities are locally introduced to the bedding protective film 51 may be used as the impurity diffusion source 511.

Other Embodiments

In any embodiment described above, the examples of adopting this invention to a top gate type TFT are explained; however, this invention may be applied to a bottom gate type TFT.

Efficacy of the Invention

As explained above, in this invention, even if hole/electron pairs due to hot carriers are formed by an increase in drain voltage in e.g., an N type TFT, these holes/electrons are recombined and then captured at a recombination center formed in a channel region. Therefore, no holes are injected from the channel region to a source region, so that the injection of electrons from the source region to the channel region resulting from such an injection of holes will not occur. As a result, there are no fluctuations in saturation current caused by such bipolar transistor behavior, thus preventing drain current in a saturation region (saturation current) from increasing along with the rise of drain voltage. Thus, even if ON-state current characteristics are improved by enhancing the degree of crystallization of a semiconductor film, the TFT itself and peripheral circuits will not be damaged by excess current, etc., thus improving reliability.

CLAIMS

1. A method of manufacturing a thin-film transistor wherein a channel region facing a gate electrode through a gate insulating film and source and drain regions connected to the channel region are formed in a semiconductor film formed on a surface of an insulating substrate, characterized in that a recombination center for capturing carriers is formed in the channel region by introducing an impurity to said channel region.
2. A method of manufacturing a thin-film transistor according to Claim 1, characterized in that said impurity is at least one kind selected from the group consisting of inert gases, metals, Group III elements, Group IV elements and Group V elements.
3. A method of manufacturing a thin-film transistor according to Claim 1 or Claim 2, characterized in that a process of introducing said impurity to said channel region is carried out by injecting the impurity from a surface side of said channel region.
4. A method of manufacturing a thin-film transistor according to Claim 3, characterized in that a process of introducing said impurity to said channel region is carried out, after a crystallization process on a semiconductor film so as to form said channel region, by injecting the impurity from a surface side of said channel region.
5. A method of manufacturing a thin-film transistor according to Claim 3, characterized in that a process of introducing said impurity to said channel region is carried out, after a crystallization process on a semiconductor film so as to form said channel region, by injecting the impurity from a surface side of said channel region before a process of forming said gate electrode on a surface side of the channel region.
6. A method of manufacturing a thin-film transistor according to Claim 3, characterized in that a process of introducing said impurity to said channel region is carried out, after said gate insulating film and said gate electrode are sequentially formed on a surface side of said channel region, by injecting the impurity from a surface side of said gate electrode before an interlayer insulating film is formed on a surface side of the gate electrode.

7. A method of manufacturing a thin-film transistor according to any of Claims 3 to 6, characterized in that an average projected range of the impurity in said process of introducing an impurity is from the center in the direction of thickness of said channel region to an interface between the channel region and the gate insulating film.
8. A method of manufacturing a thin-film transistor according to any of Claims 3 to 6, characterized in that an average projected range of the impurity in said process of introducing an impurity is from the center in the direction of thickness of said channel region to an interface between the channel region and a layer located on said substrate side.
9. A method of manufacturing a thin-film transistor according to Claim 1 or Claim 2, characterized in that a process of introducing said impurity to said channel region is carried out by impurity diffusion from an impurity diffusion source arranged at a lower layer side of said channel region.
10. A method of manufacturing a thin-film transistor according to Claim 9, characterized in that said impurity diffusion is carried out in a crystallization process on a semiconductor film so as to form said channel region.
11. A method of manufacturing a thin-film transistor according to Claim 4, Claim 5 or Claim 10, characterized in that said crystallization process is laser annealing on a semiconductor film so as to form said channel region.
12. A method of manufacturing a thin-film transistor according to Claim 1 or Claim 11, characterized in that each process carried out after introducing said impurities to said channel region is carried out at a temperature below 400°C.
13. A method of manufacturing a thin-film transistor according to Claim 1 or Claim 11, characterized in that each process carried out after introducing said impurities to said channel region is carried out at a temperature below 300°C.

ABSTRACT

In a TFT 10, a channel region 15 facing a gate electrode 14 through a gate insulating film 12, a source electrode 16 connected to the channel region 15 and a drain region 17 connected to the channel region 15 on the side opposite this source region 16 are formed in a polycrystal semiconductor film 100 that was patterned in island forms. In the channel region 15, a recombination center 150 is formed for capturing a small number of carriers (holes) by introducing impurities such as inert gases, metals, Group III elements, Group IV elements and Group V elements after a crystallization process is carried out on a semiconductor film 100. The invention thus provides an arrangement restraining bipolar transistor type behavior, to stabilize saturation current and to provide a TFT that can improve reliability.

Fig. 1

Figure.1

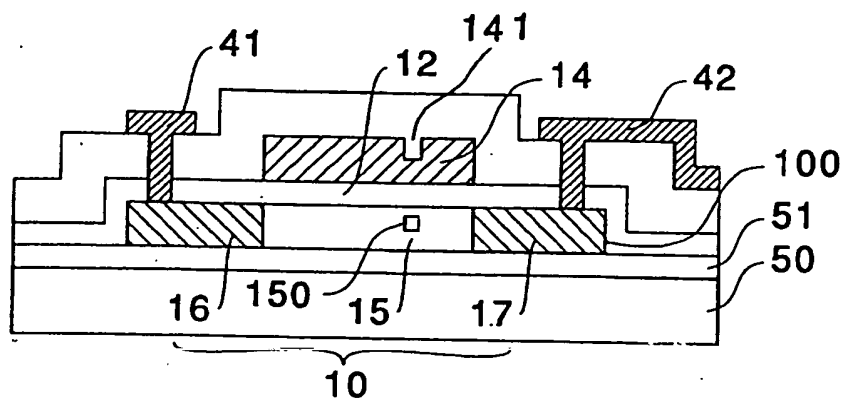


Figure.2

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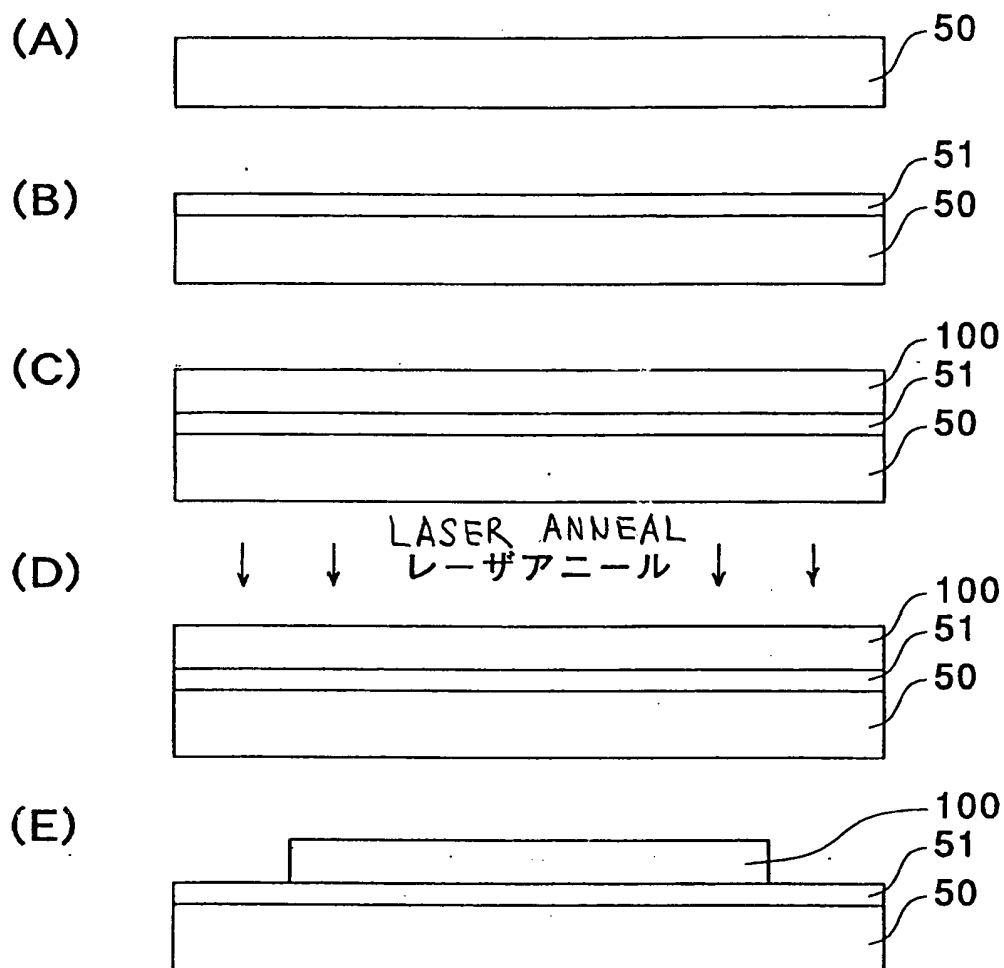


Figure.3

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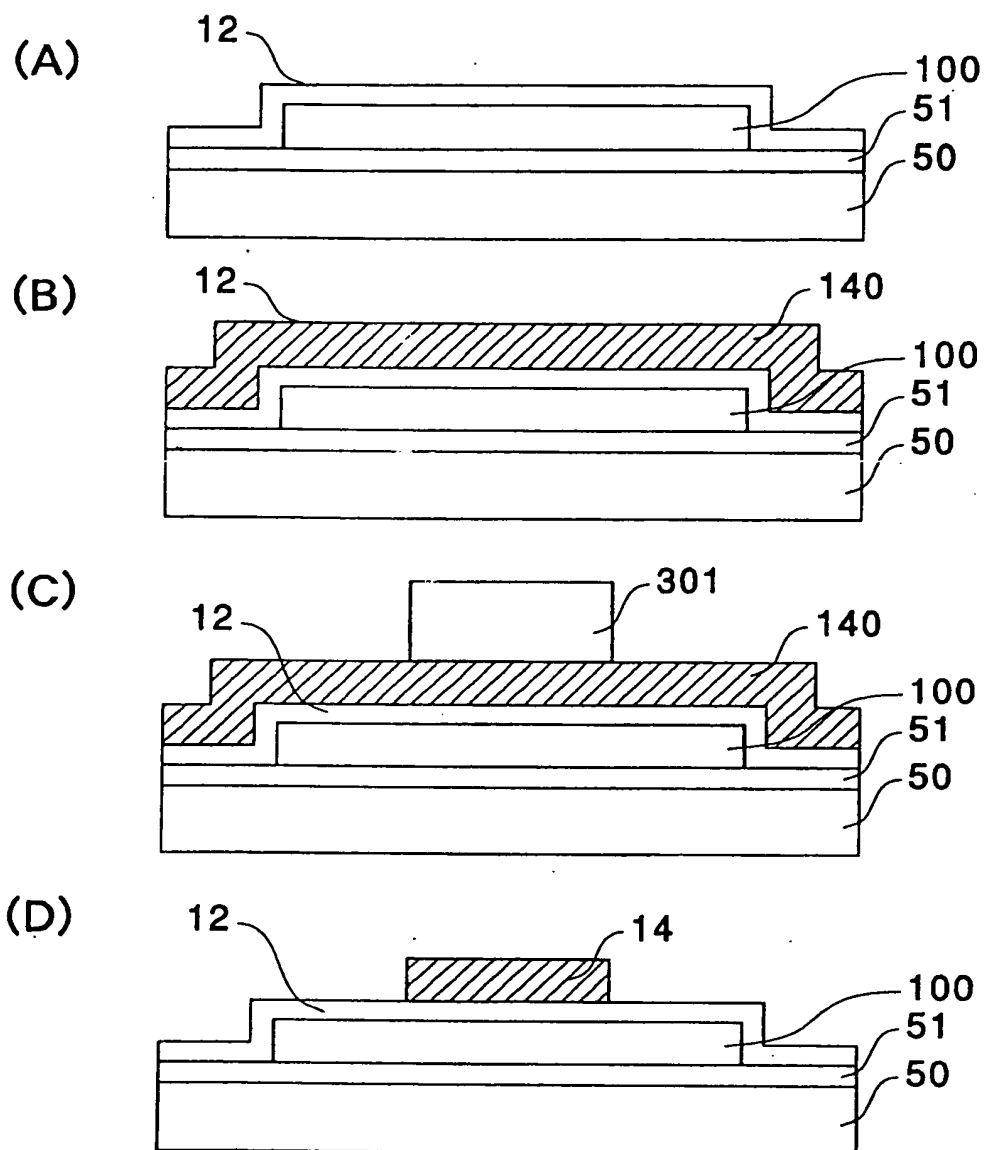


Figure 4

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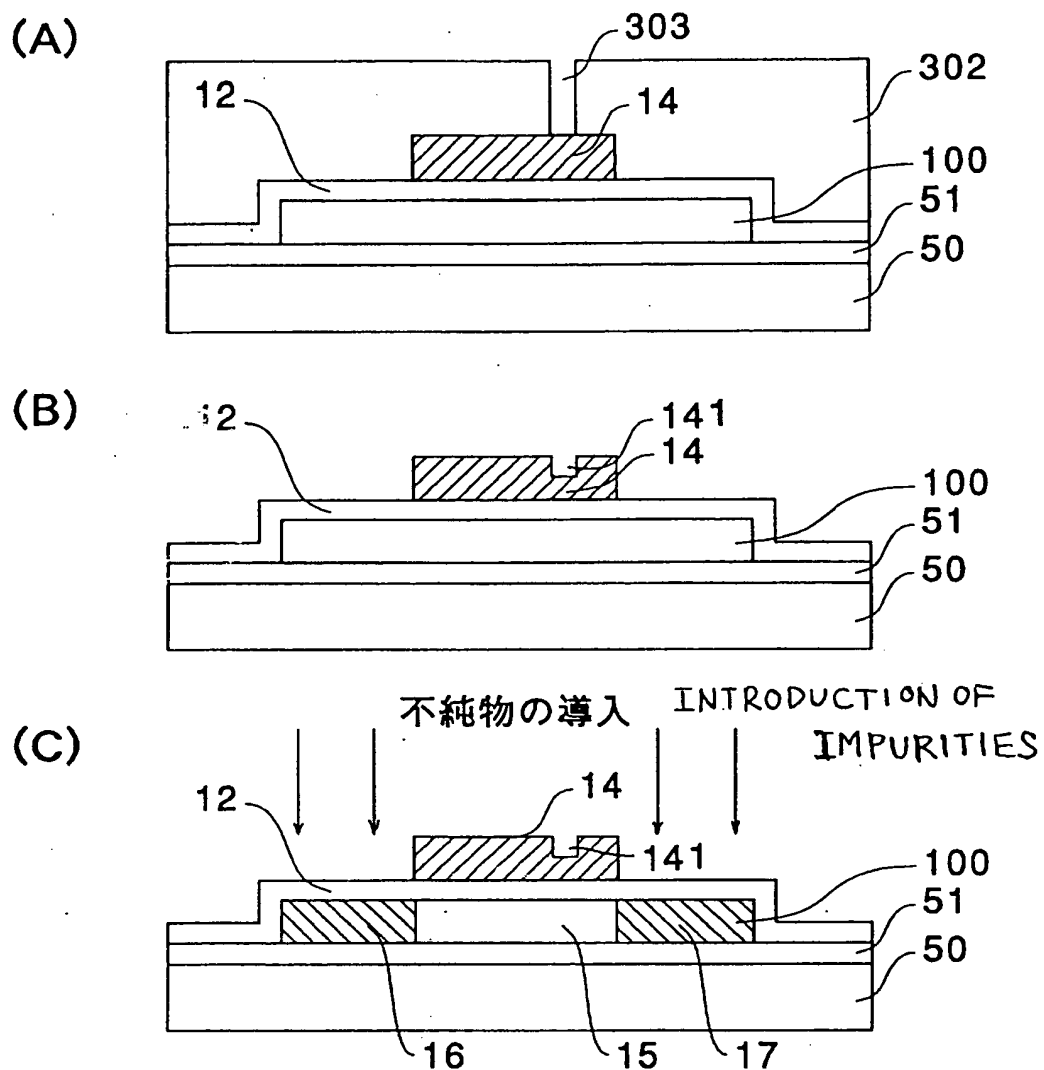
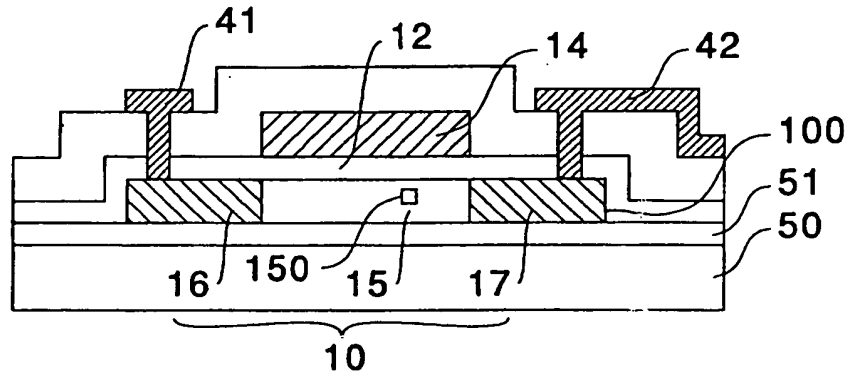


Figure.5

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Figure. 6

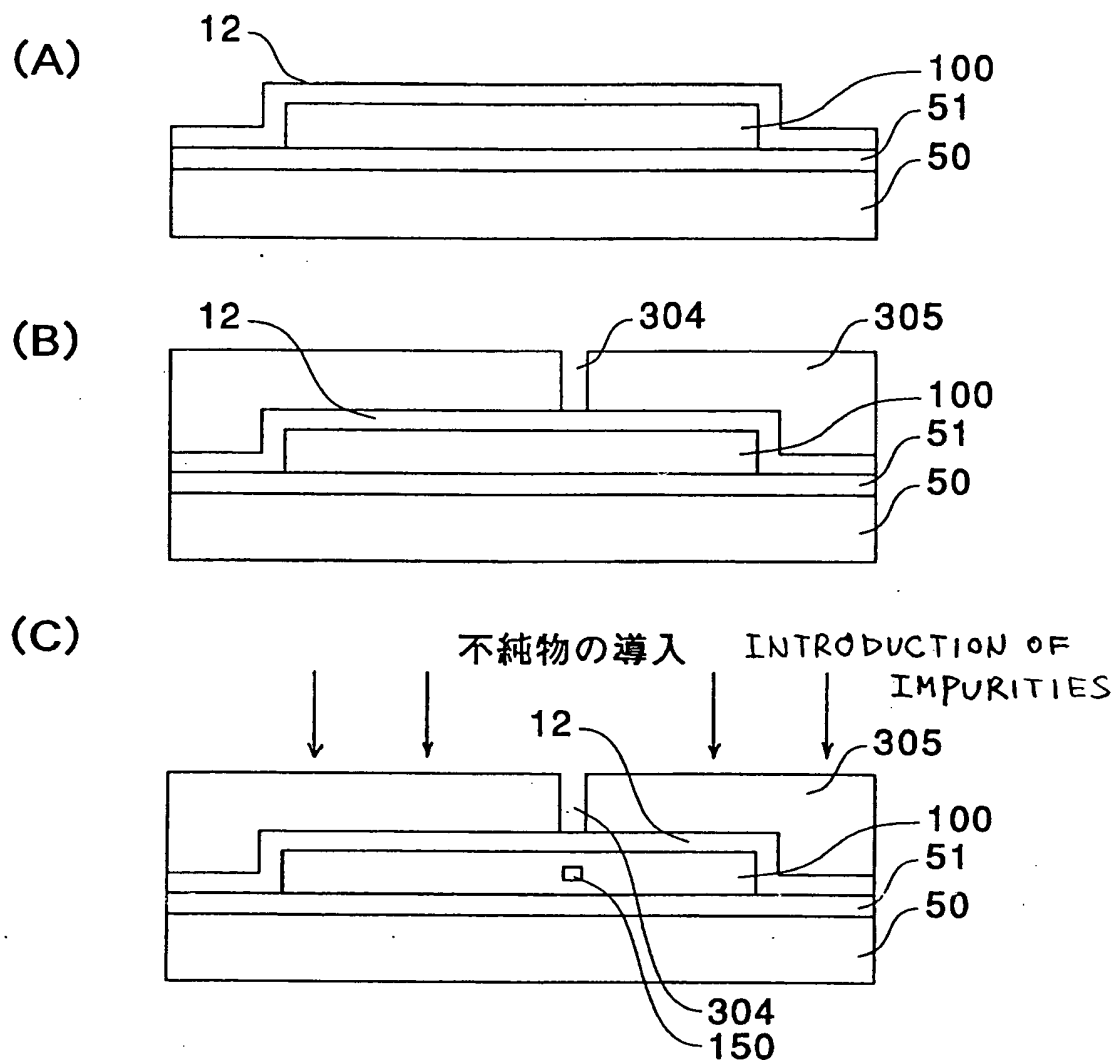


Figure. 7

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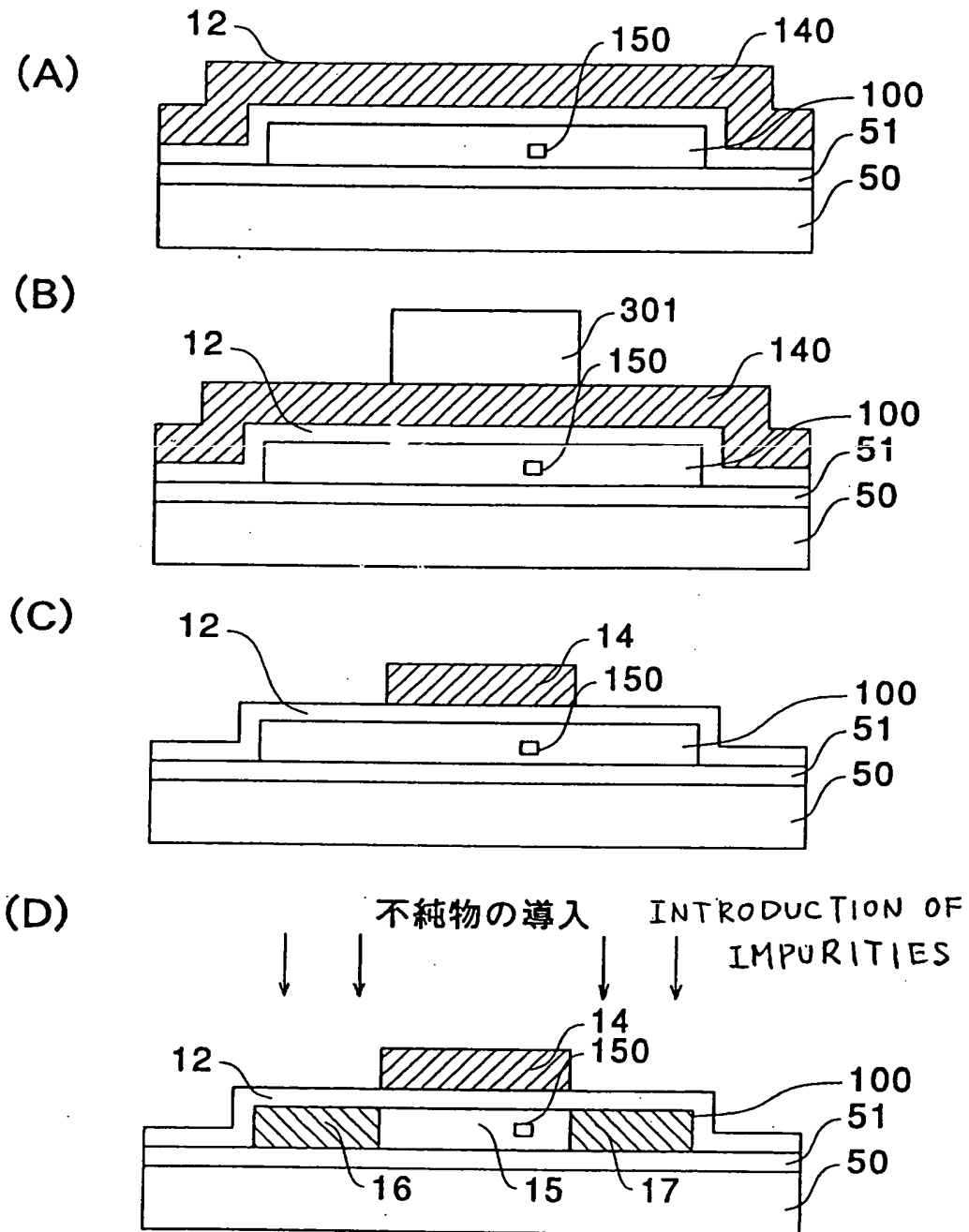


Figure. 8

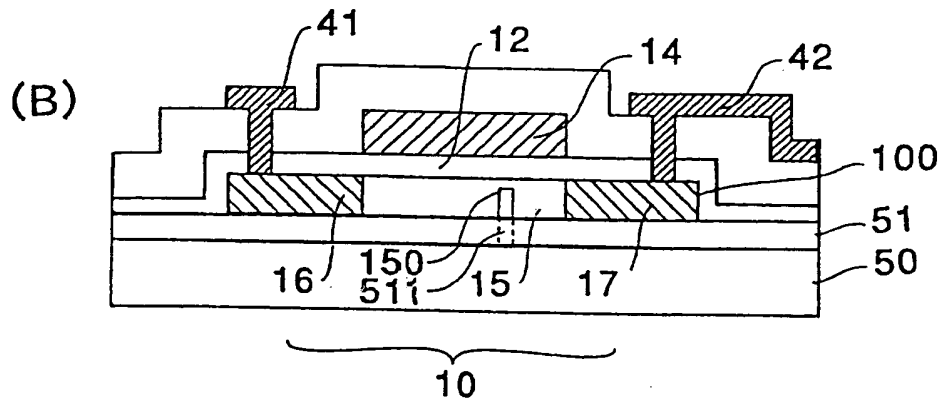
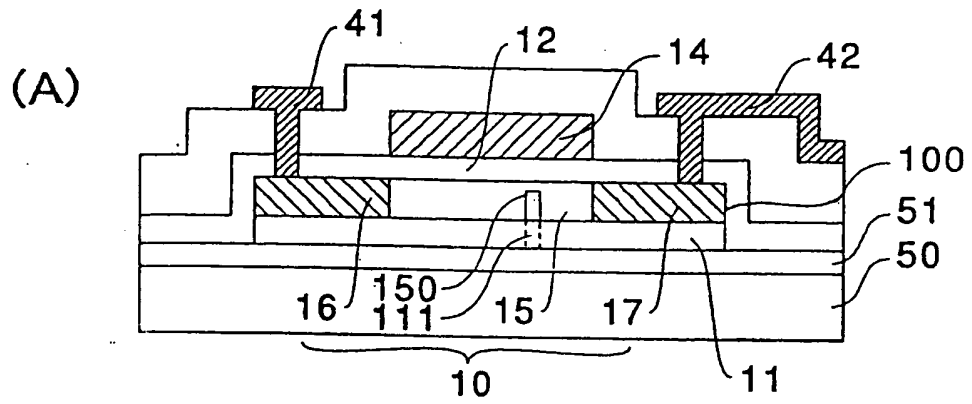
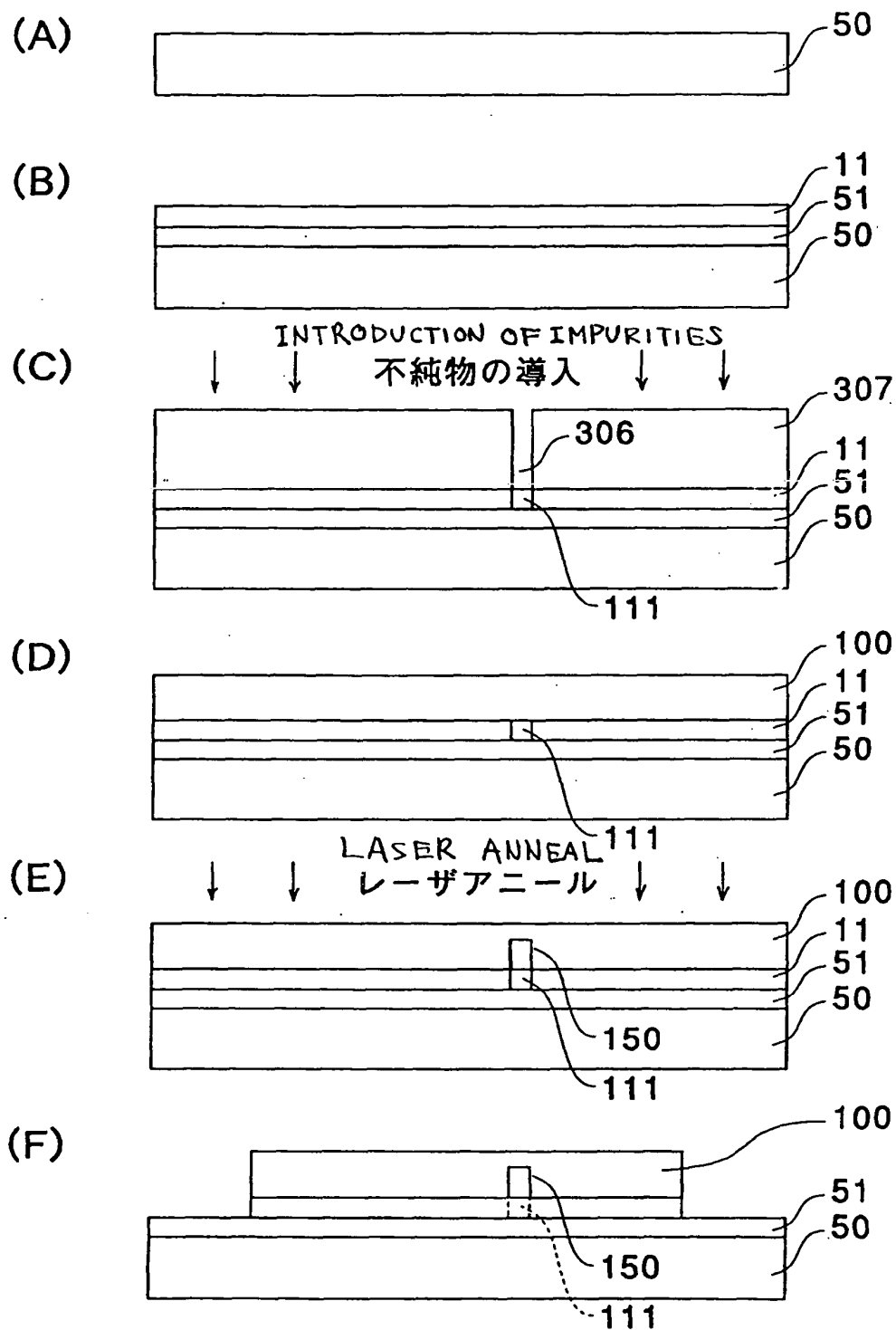


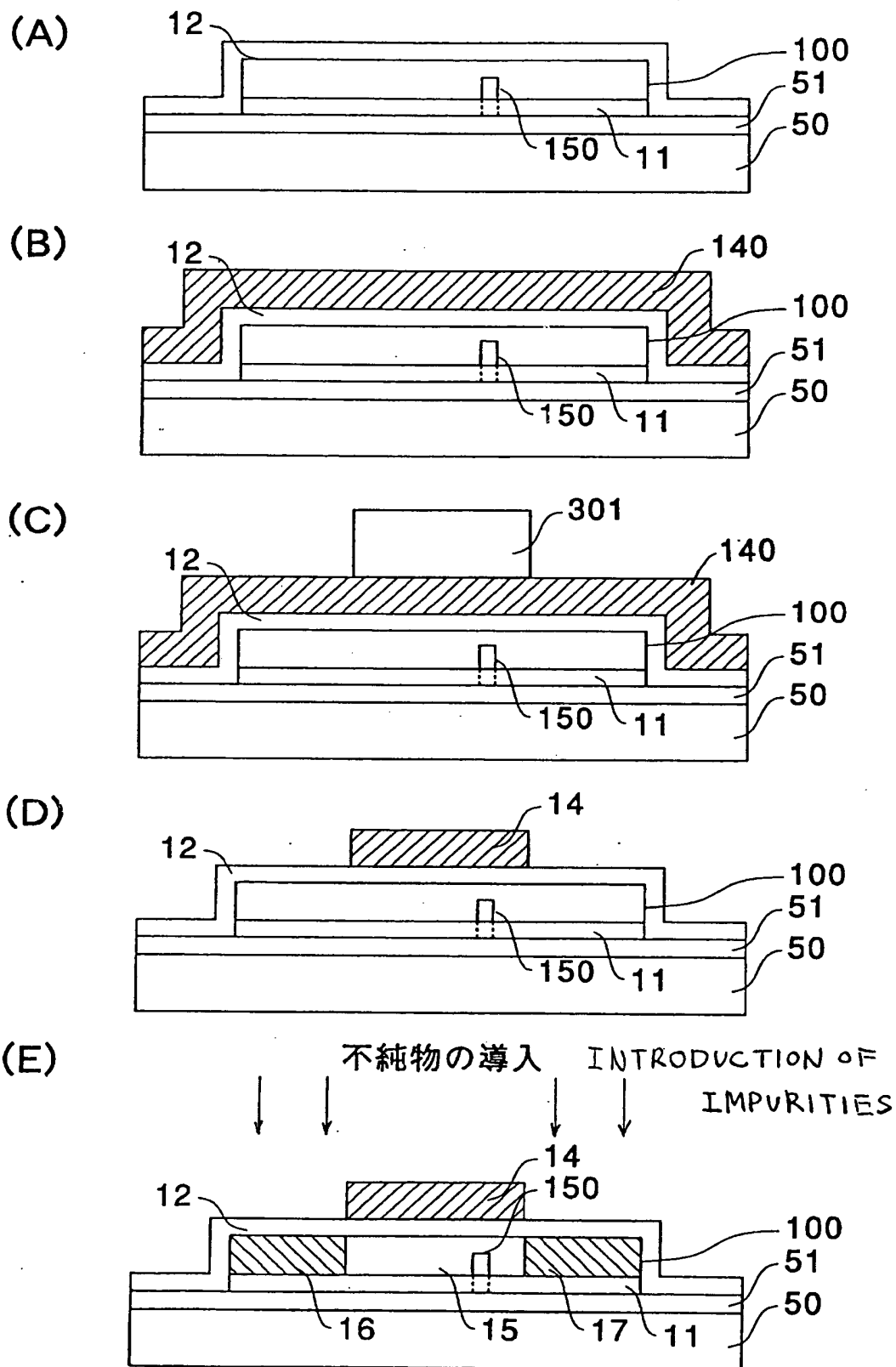
Figure.9

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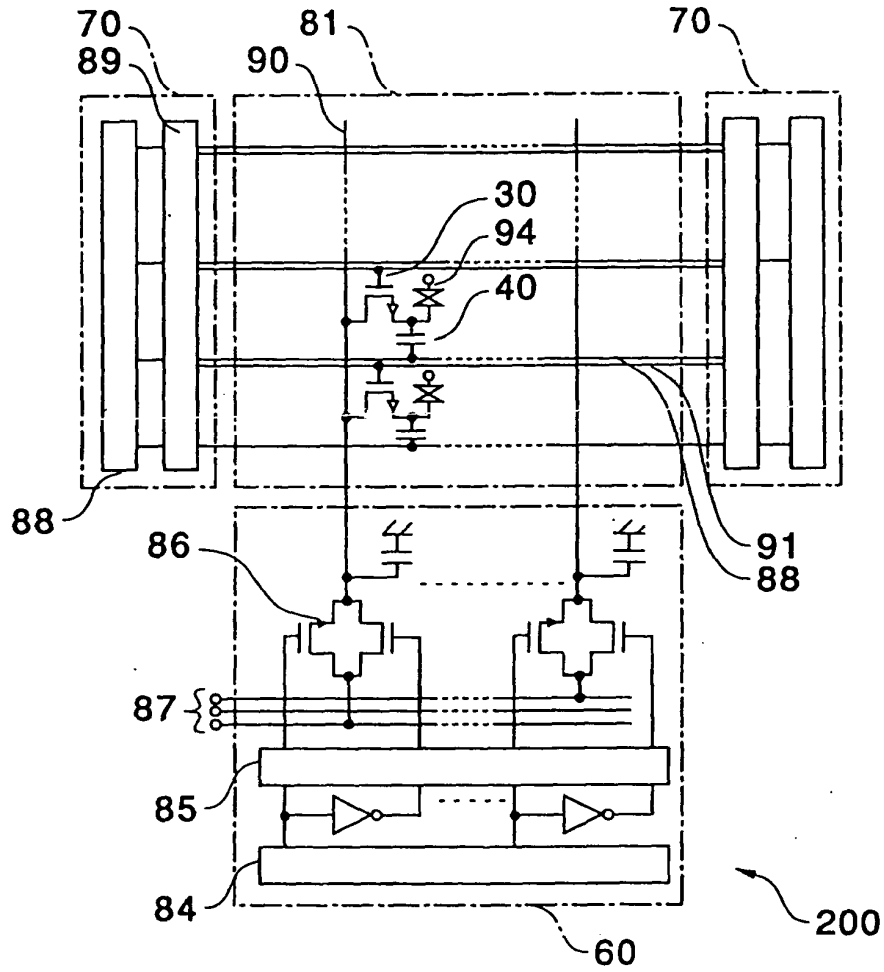
Figure 10



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Figure. 11

(A)



(B)

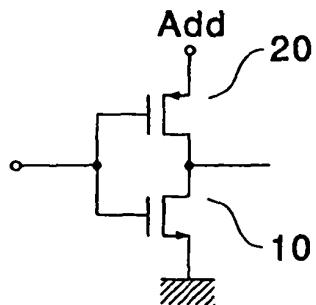


Figure 12

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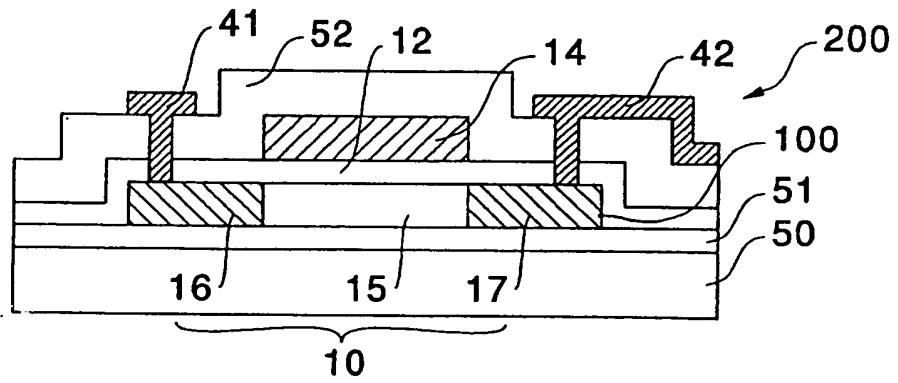
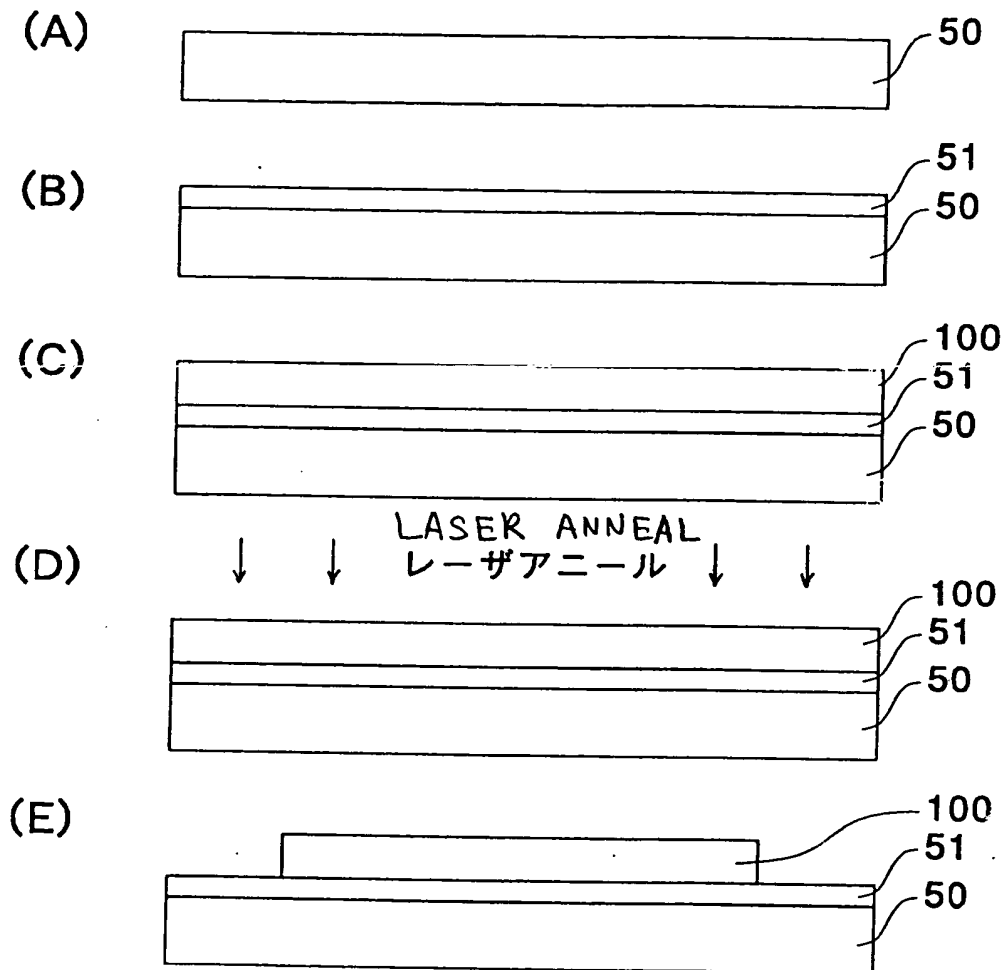


Figure.13

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Figure.14

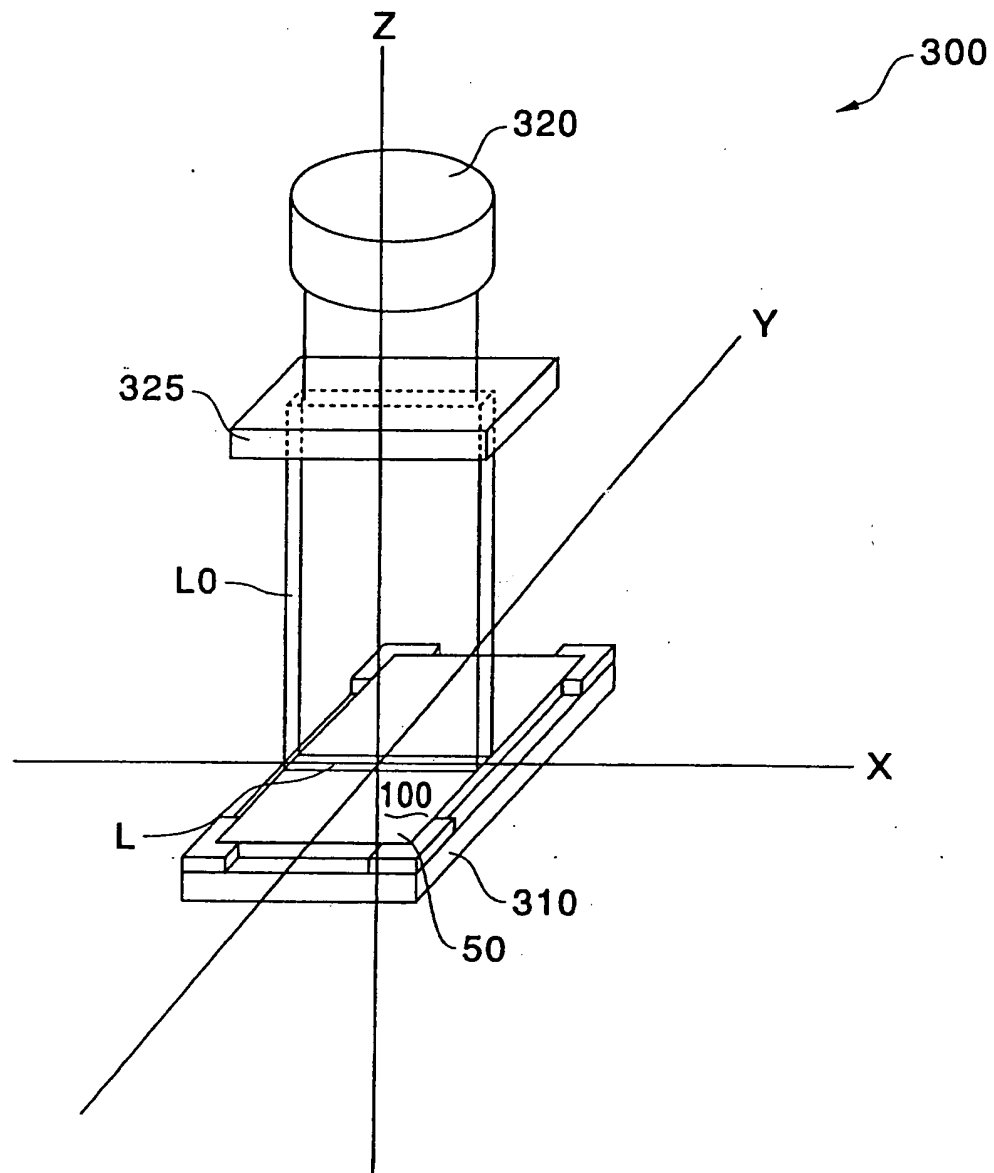
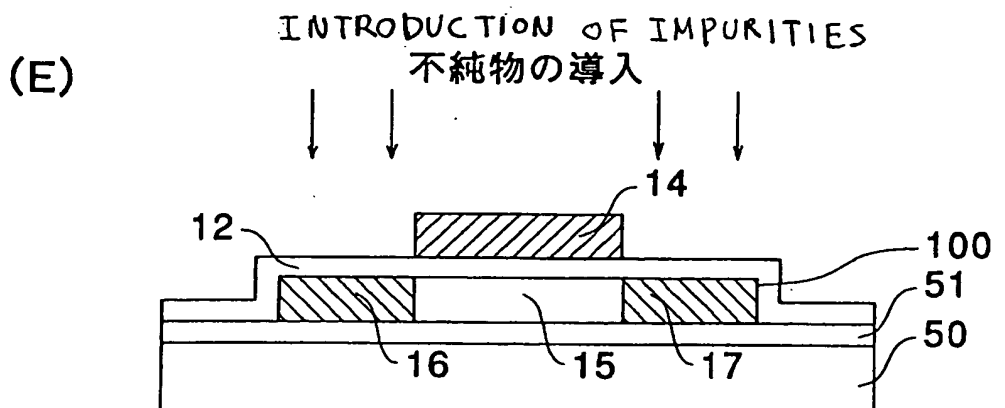
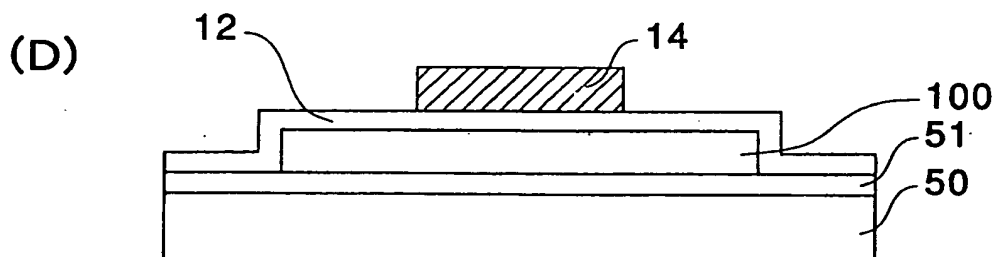
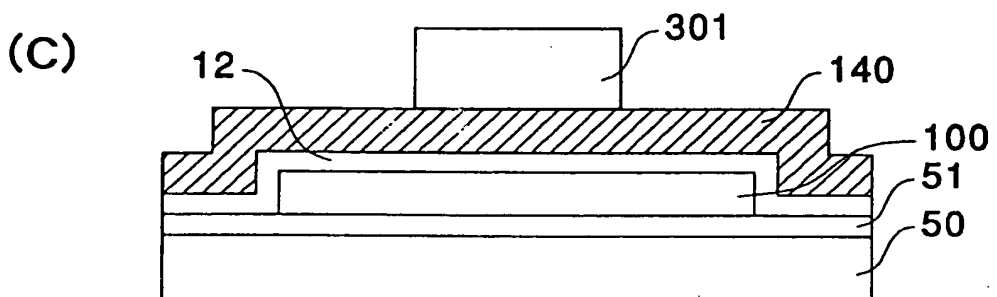
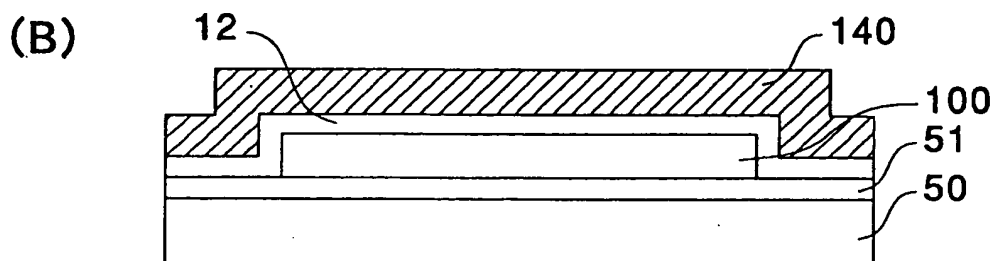
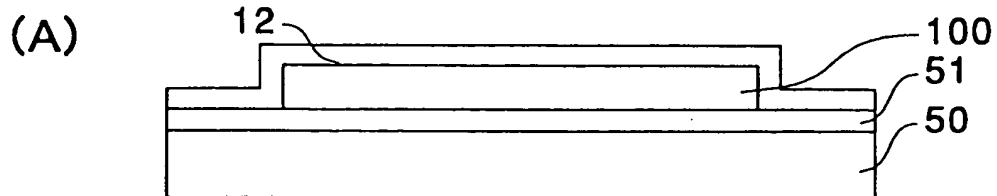


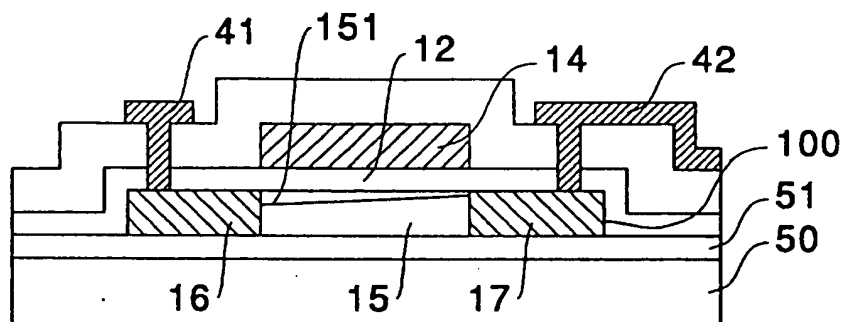
Figure 15



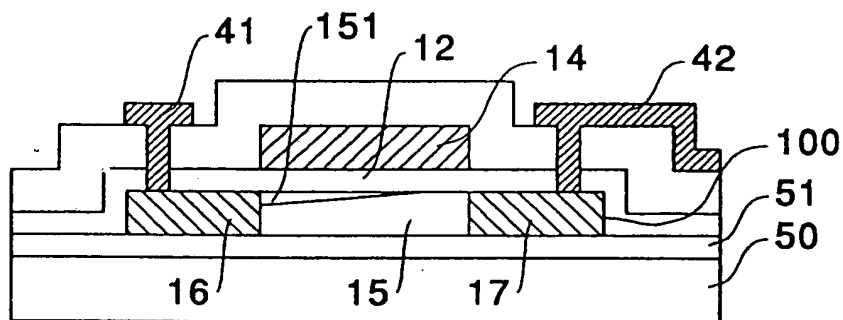
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/ 17

Figure 16

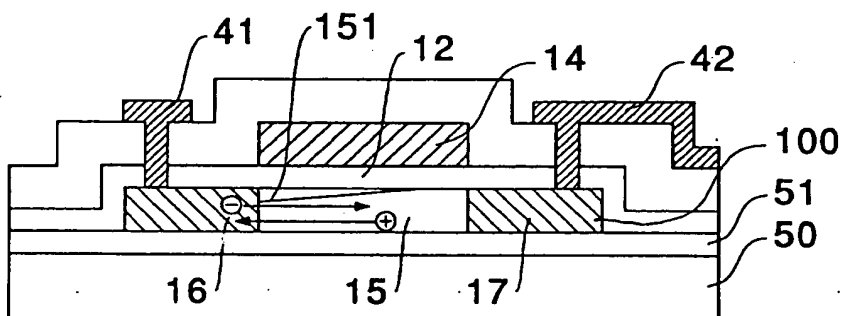
(A)



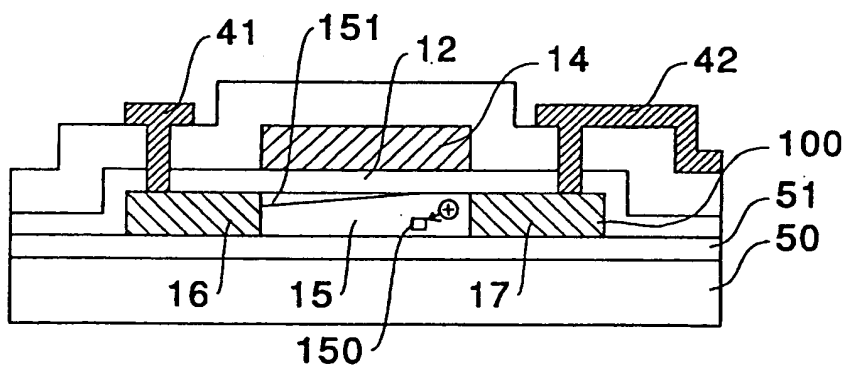
(B)



(C)



(D)



17
/17

Figure. 17

